XD/XL3842 DIP8/SOP8,XD/XL2842 DIP8/SOP8
XD/XL2843 DIP8/SOP8,XD/XL3843 DIP8/SOP8

The 3842-2842-3843-2843 series are high performance fixed frequency current mode controllers. They are specifically designed for Off−Line and DC−DC converter applications offering the designer a cost−effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

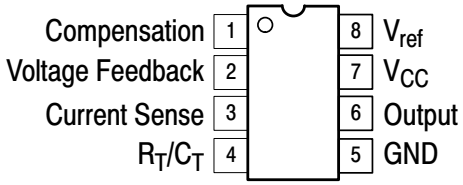
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle−by−cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

The 3842-2842 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off−line converters. The 3843-2843 is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

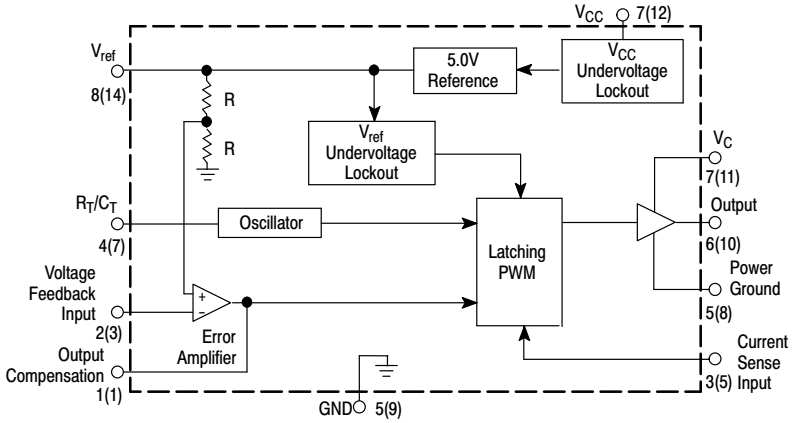
Features

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle−By−Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- This is a Pb−Free and Halide−Free Device

PIN CONNECTIONS



(Top View)



括号中的管脚编号用于D后缀SOIC−14封装。SOIC−14封装本司暂无生产

Figure 1. Simplified Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec)	V_{CC}, V_C	30	V
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Voltage Feedback, V_{ref} and Rt/Ct Inputs	V_{in}	− 0.3 to + 5.5	V
Compensation	V_{comp}	− 0.3 to + 7.2	V
Output	V_o	− 0.3 to V_{CC} or V_C + 0.3	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D1 Suffix, Plastic Package, SOIC−8 Case 751 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction−to−Air N Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 702 178 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature 3842-3843-2842-2843	T_A	0 to 70 − 25 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC Standard JESD22-A114B
   Machine Model Method 200 V per JEDEC Standard JESD22-A115-A
2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 3], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

Characteristics	Symbol	2842 2843			3842 3843			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature 2842 2843	V_{ref}	 4.9 4.82	 – –	 5.1 5.18	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	–180	– 30	– 85	–180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high} T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)	f_{OSC}	 49 48 225	 52 – 250	 55 56 275	 49 48 225	 52 – 250	 55 56 275	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature, T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V) T_J = 25°C, T_A = T_{low} to T_{high} 2842 3842 2843 3843	I_{dischg}	 7.8 7.5 –	 8.3 – –	 8.8 8.8 –	 7.8 7.6 7.2	 8.3 – –	 8.8 8.8 8.8	mA
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V) 2842 2843	V_{FB}	 2.45 2.42	 2.5 2.5	 2.55 2.58	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current Sink (V_O = 1.1 V, V_{FB} = 2.7 V) Source (V_O = 5.0 V, V_{FB} = 2.3 V)	 I_{Sink} I_{Source}	 2.0 – 0.5	 12 –1.0	 – –	 2.0 – 0.5	 12 –1.0	 – –	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V) 2842 3842 2843 3843	 V_{OH} V_{OL}	 5.0 – –	 6.2 0.8 –	 – 1.1 –	 5.0 – –	 6.2 0.8 0.8	 – 1.1 1.2	V

3. Adjust V_{CC} above the Startup threshold before setting to 15 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for 3842,3843; –25°C for 2842,2843; –40°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 7], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 8], unless otherwise noted.)

Characteristics	Symbol	2842 2843 Min	2842 2843 Typ	2842 2843 Max	3842 3843 Min	3842 3843 Typ	3842 3843 Max	Unit
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 5 and 6)	A_V							V/V
2843 2842 3842 3843		2.85	3.0	3.15	2.85	3.0	3.15	
		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 5)	V_{th}							V
2843 2842 3842 3843		0.9	1.0	1.1	0.9	1.0	1.1	
		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V, Note 5)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA) 2843 2842		–	1.6	2.2	–	1.6	2.2	
3842 3843		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA) 2843 2842	V_{OH}	13	13.5	–	13	13.5	–	
3842 3843		–	–	–	12.9	13.5	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold (V_{CC})	V_{th}							V
2843 2842		15	16	17	14.5	16	17.5	
3842 3843		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On (V_{CC})	$V_{CC(min)}$							V
2843 2842		9.0	10	11	8.5	10	11.5	
3842 3843		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum 2843 2842 3842 3843	$DC_{(max)}$	94	96	–	94	96	–	
		–	–	–	93	96	–	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	$I_{CC} + I_C$							mA
Startup (V_{CC} = 6.5 V for 3843 2843		–	0.3	0.5	–	0.3	0.5	
V_{CC} 14 V for 2842, BV)								
(Note 7)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

5. This parameter is measured at the latch trip point with V_{FB} = 0 V.
6. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$
7. Adjust V_{CC} above the Startup threshold before setting to 15 V.
8. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible. T_{low} = 0°C for 3842 3843; –25°C for 2842 2843; –40°C

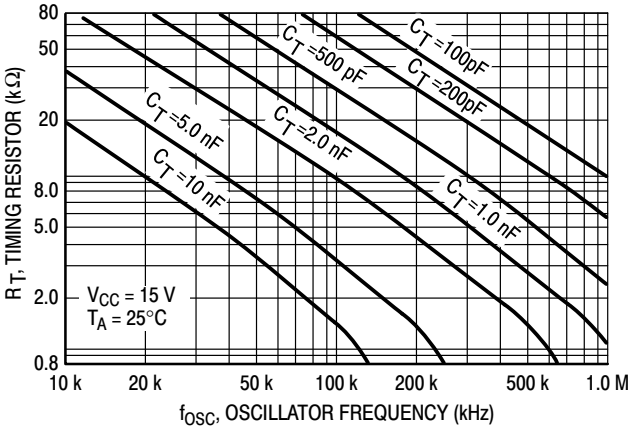


Figure 2. Timing Resistor versus Oscillator Frequency

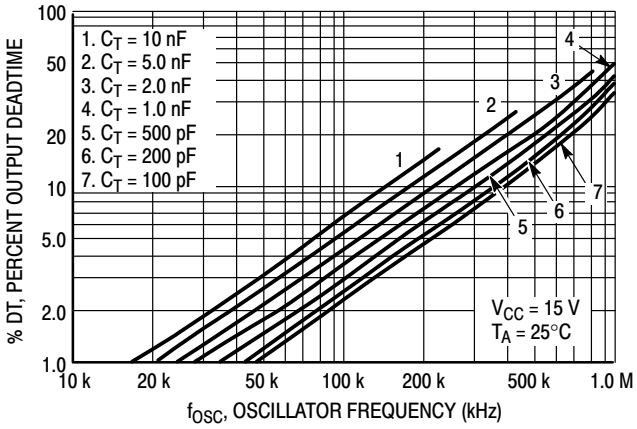


Figure 3. Output Deadtime versus Oscillator Frequency

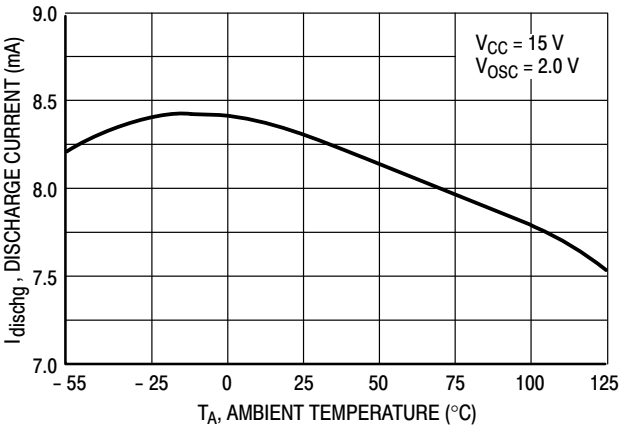


Figure 4. Oscillator Discharge Current versus Temperature

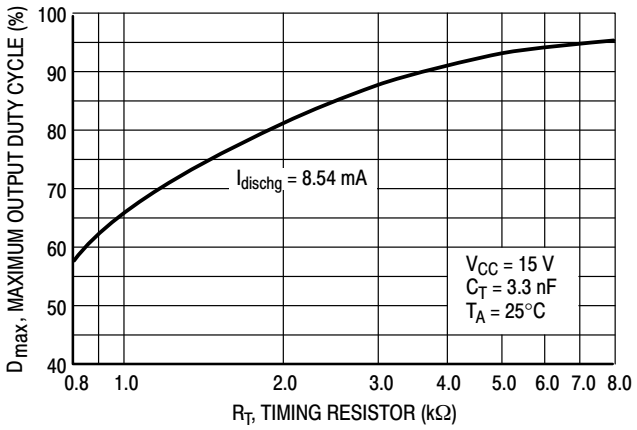


Figure 5. Maximum Output Duty Cycle versus Timing Resistor

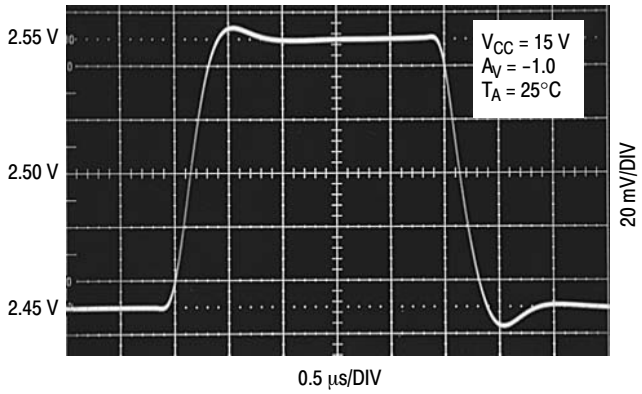


Figure 6. Error Amp Small Signal Transient Response

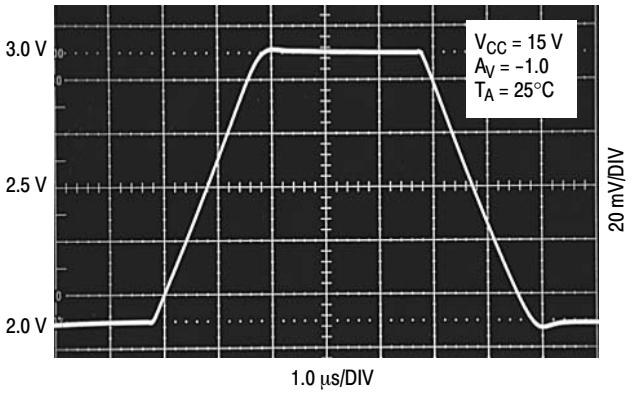


Figure 7. Error Amp Large Signal Transient Response

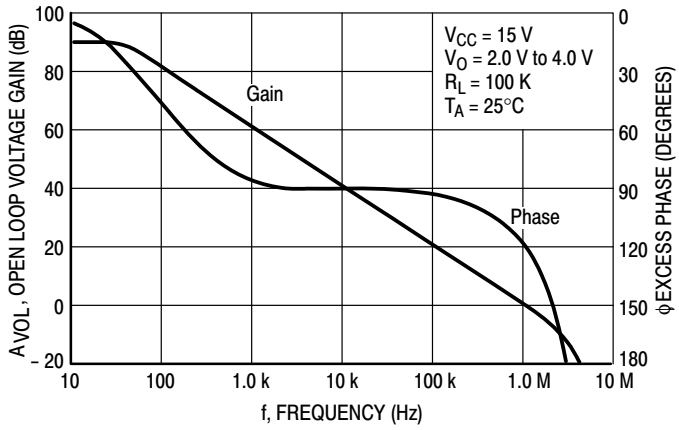


Figure 8. Error Amp Open Loop Gain and Phase versus Frequency

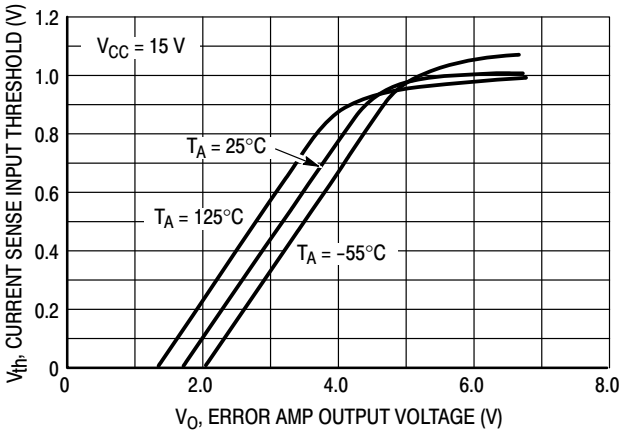


Figure 9. Current Sense Input Threshold versus Error Amp Output Voltage

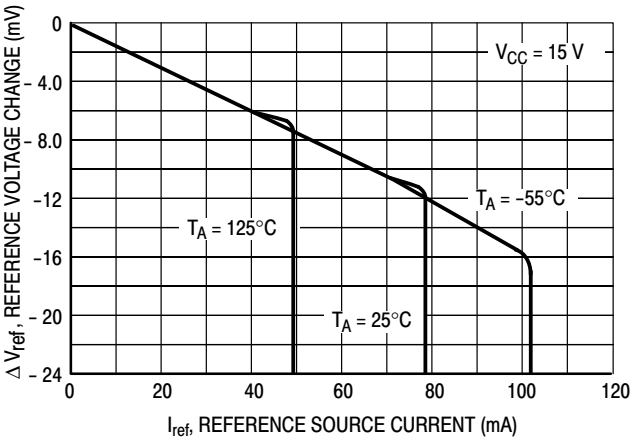


Figure 10. Reference Voltage Change versus Source Current

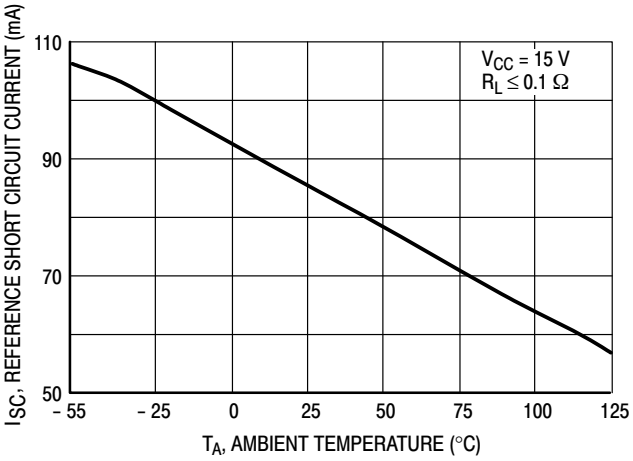


Figure 11. Reference Short Circuit Current versus Temperature

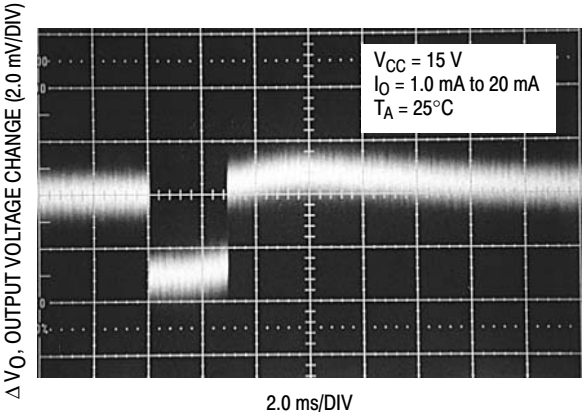


Figure 12. Reference Load Regulation

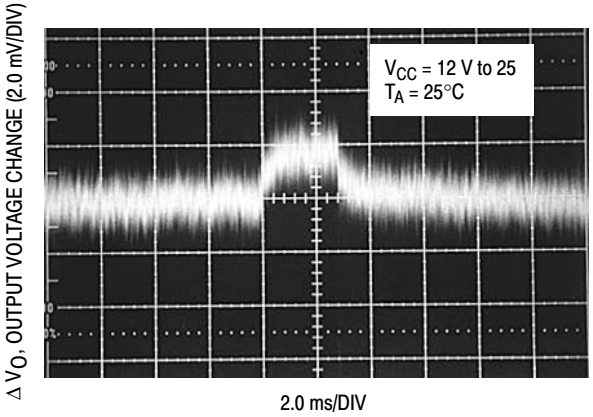


Figure 13. Reference Line Regulation

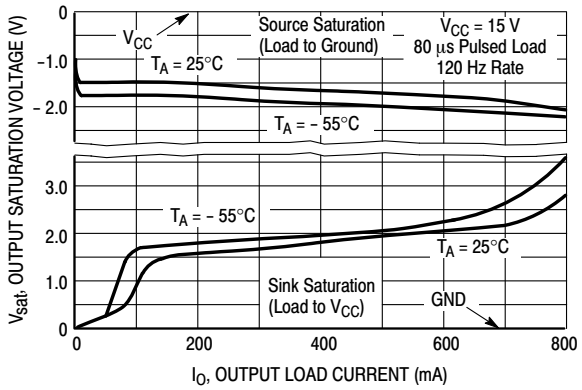


Figure 14. Output Saturation Voltage versus Load Current

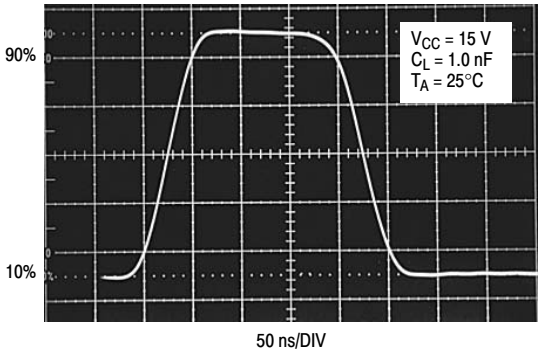


Figure 15. Output Waveform

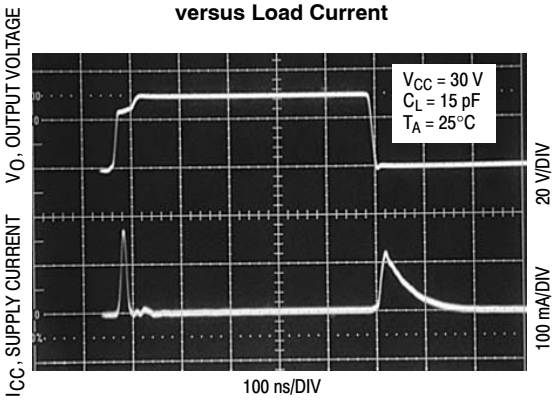


Figure 16. Output Cross Conduction

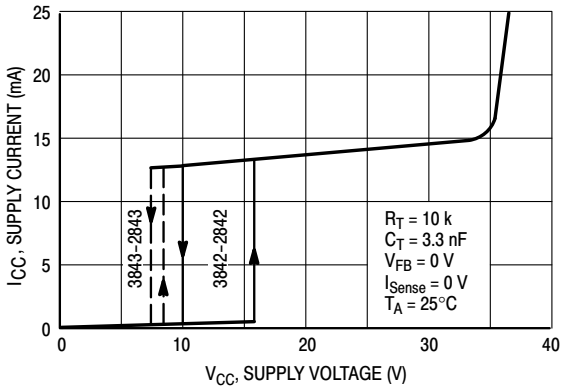


Figure 17. Supply Current versus Supply Voltage

PIN FUNCTION DESCRIPTION

8−Pin	14−Pin	Function	Description
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		GND	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	GND	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 8). The non−inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is −2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 33). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non−inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft−start interval (Figures 25, 26). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The 3842, 3843 operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle−by−cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground−referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 24. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 28).

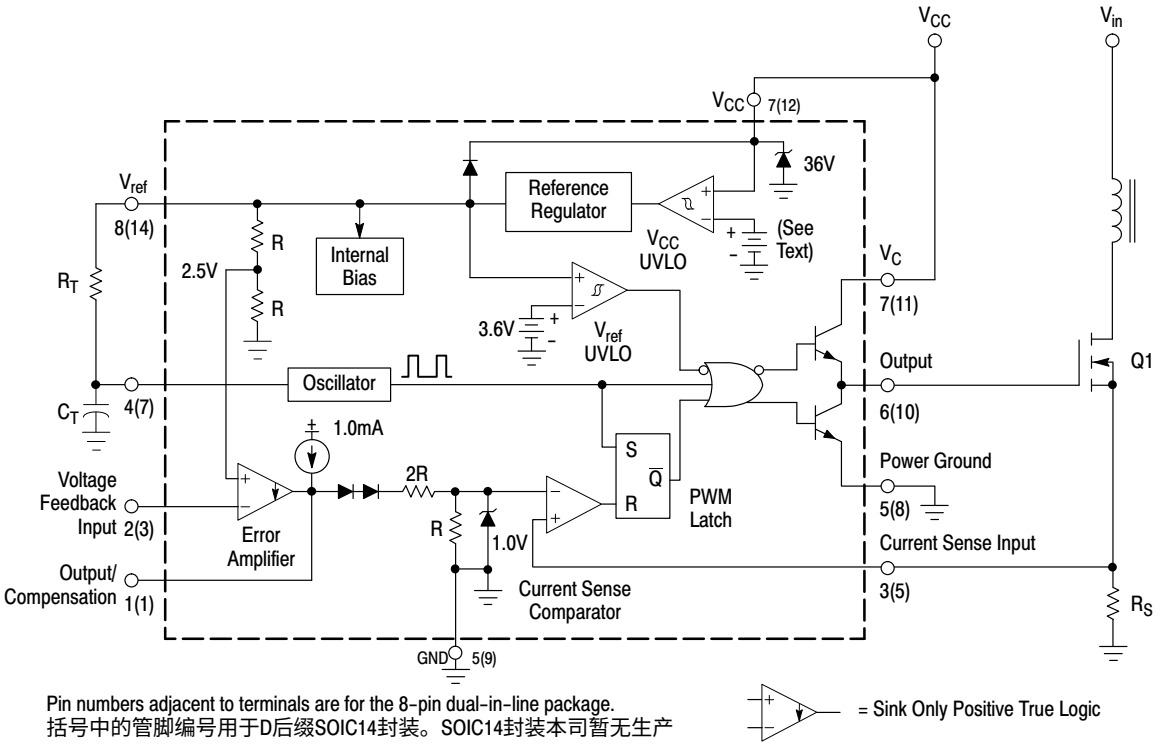


Figure 19. Representative Block Diagram

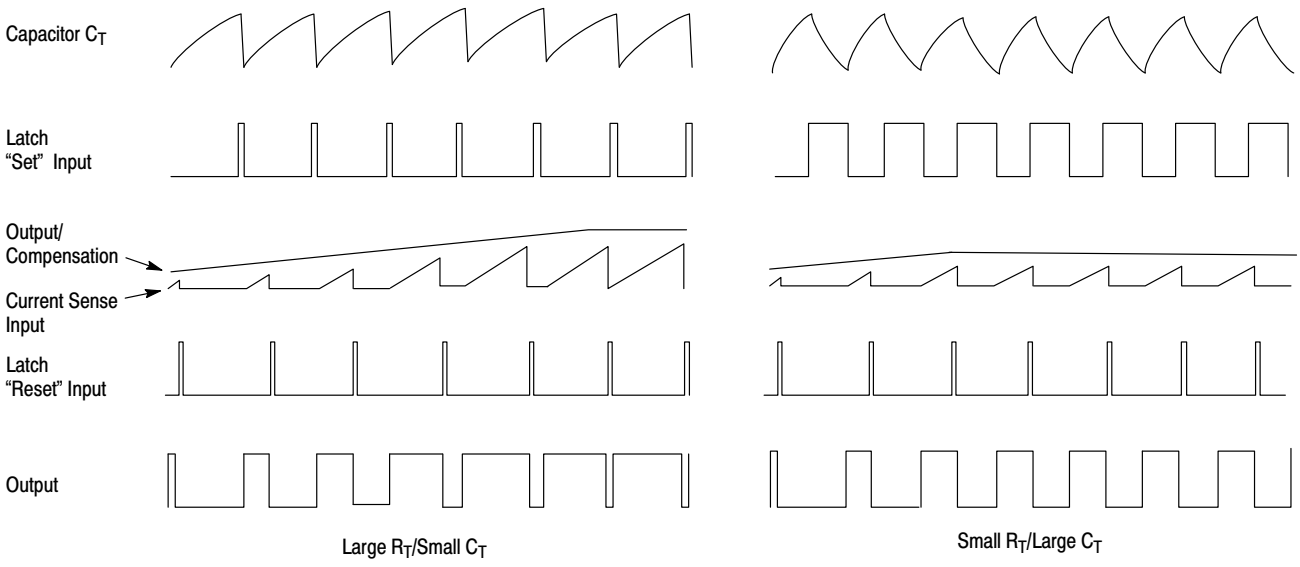


Figure 20. Timing Diagram

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built−in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the X842, and 8.4 V/7.6 V for the X843. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the X842 makes it ideally suited in off−line converter applications where efficient bootstrap startup techniques are required (Figure 35). The X843 is intended for lower voltage DC−to−DC converter applications. A 36 V Zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage (V_{CC}) for the X842 is 11 V and 8.2 V for the X843.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull−down resistor.

The SOIC−14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A Zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 27 shows proper power and control ground connections in a current−sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the 284X, and ±2.0% on the 384X. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short−circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire−wrap or plug−in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse−width jitter. This is usually caused by excessive noise pick−up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low−current signal and high−current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise−generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 21A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn−on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)\,(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn−on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 21B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 34).

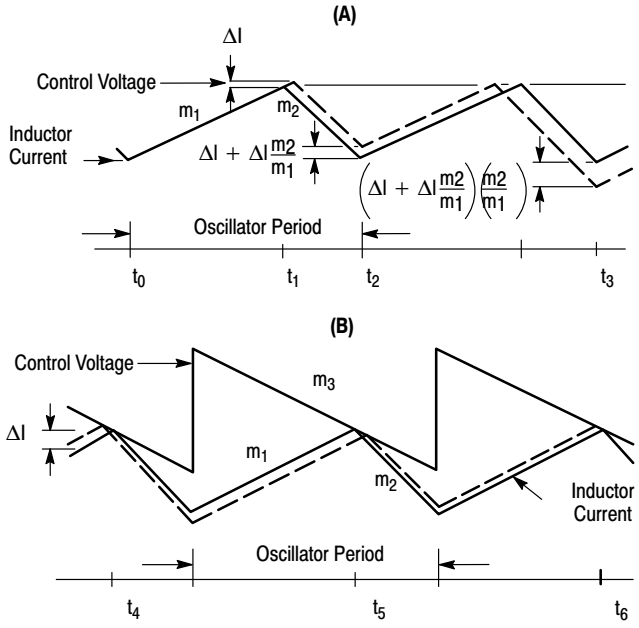
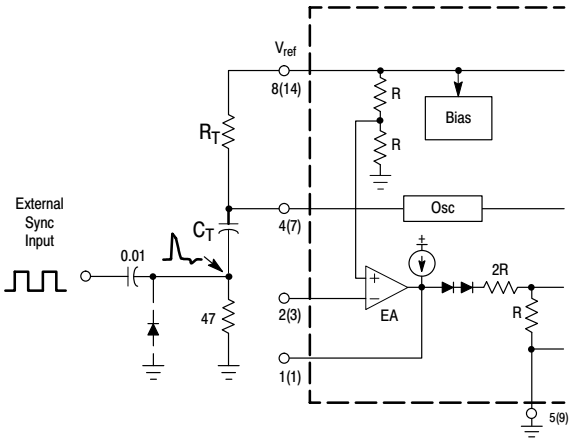


Figure 21. Continuous Current Waveforms



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 22. External Clock Synchronization

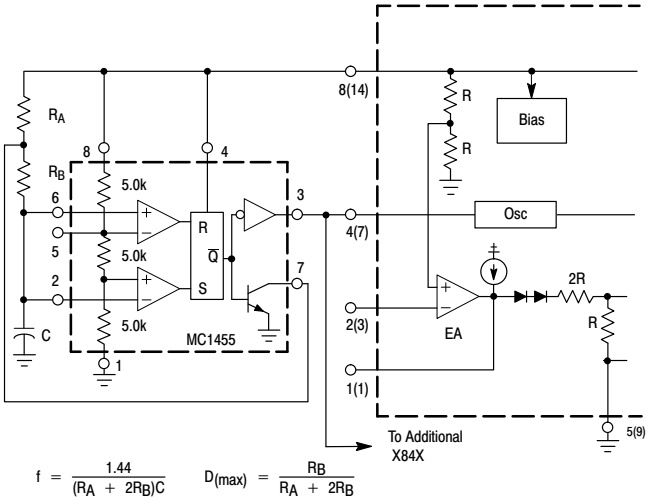


Figure 23. External Duty Cycle Clamp and Multi−Unit Synchronization

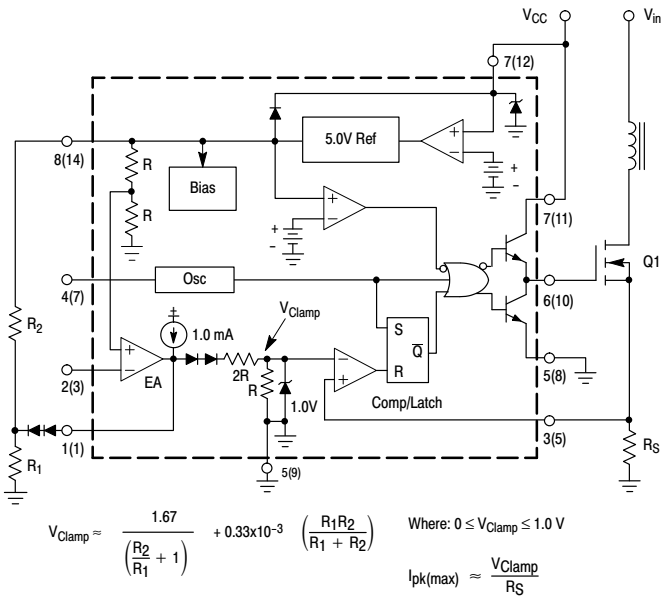


Figure 24. Adjustable Reduction of Clamp Level

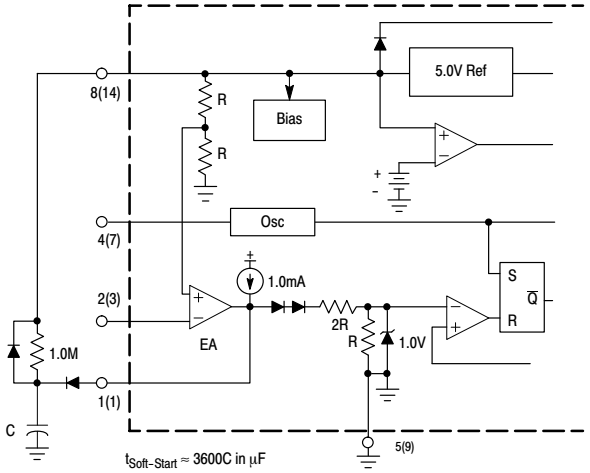


Figure 25. Soft−Start Circuit

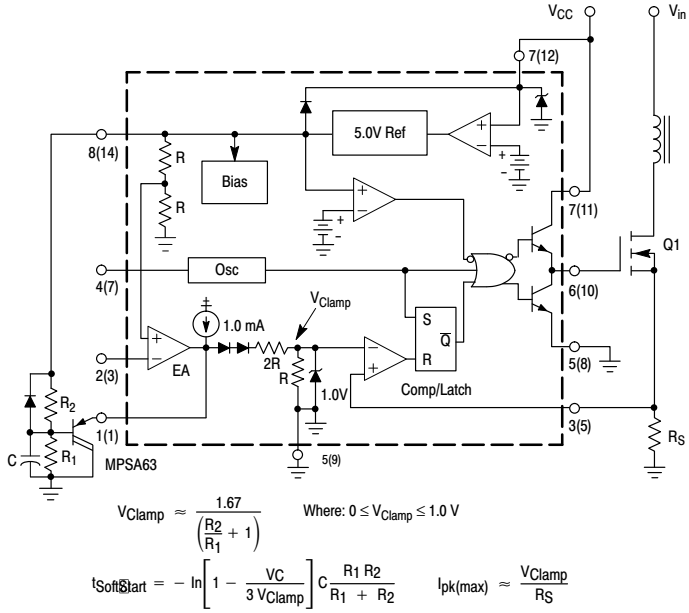
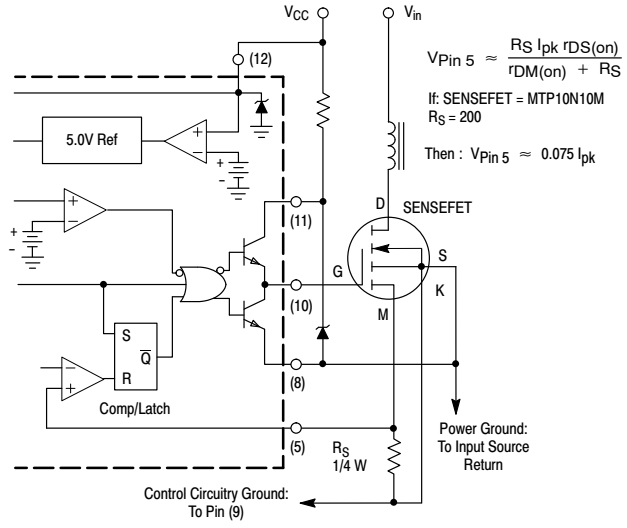
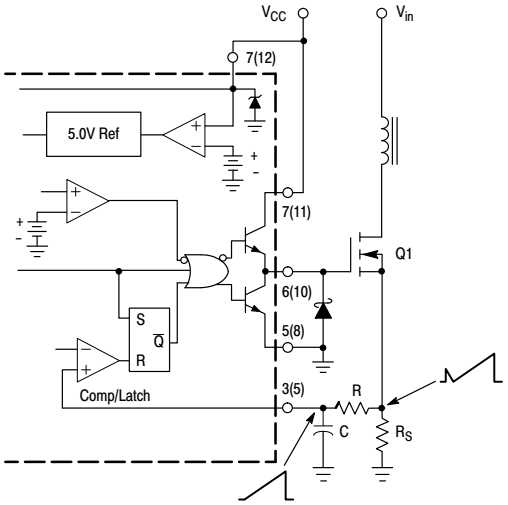


Figure 26. Adjustable Buffered Reduction of Clamp Level with Soft−Start



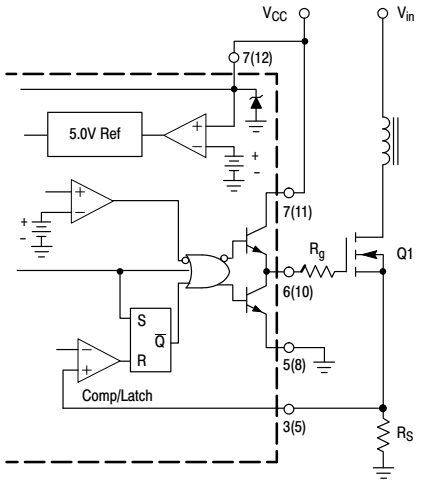
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over−current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 24 and 26.

Figure 27. Current Sensing Power MOSFET



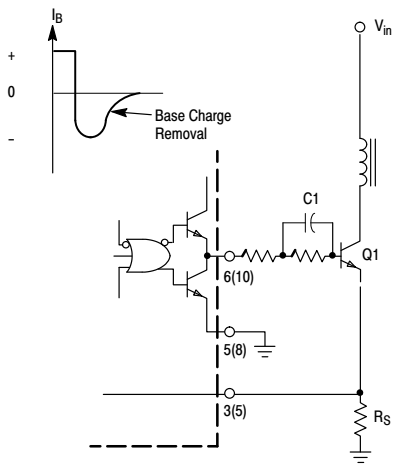
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 28. Current Waveform Spike Suppression



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate−source circuit.

Figure 29. MOSFET Parasitic Oscillations



The totem pole output can furnish negative base current for enhanced transistor turn−off, with the addition of capacitor C_1.

Figure 30. Bipolar Transistor Drive

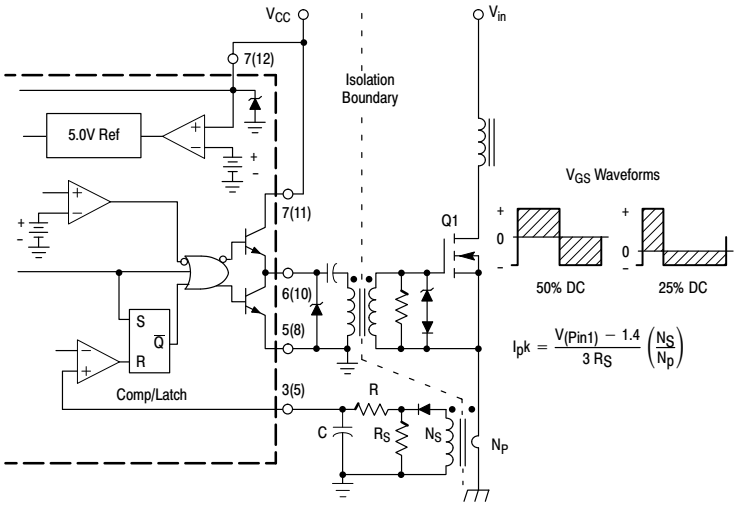
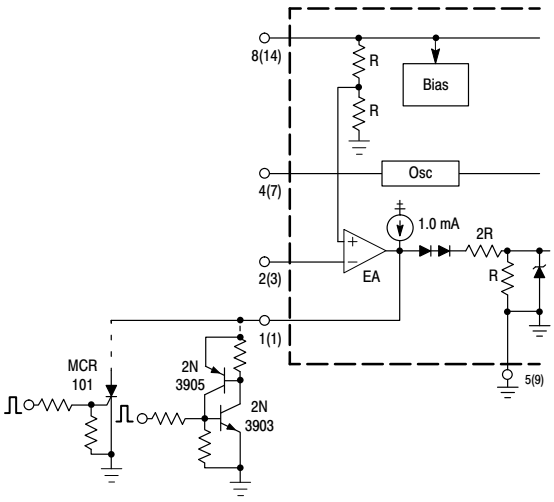
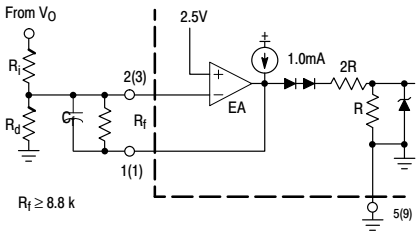


Figure 31. Isolated MOSFET Drive

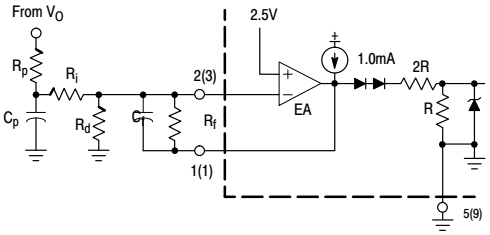


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 32. Latched Shutdown

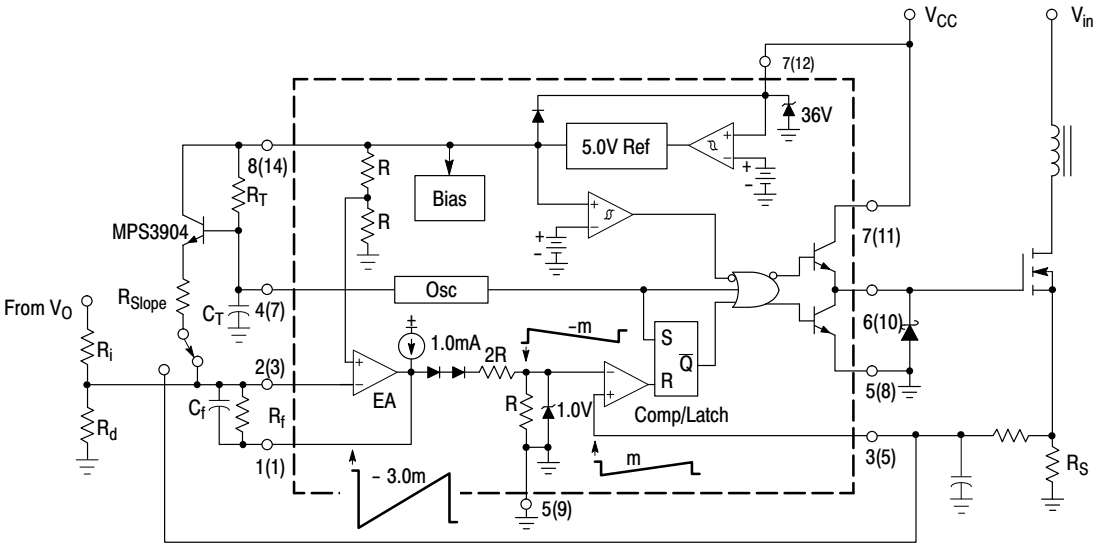


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



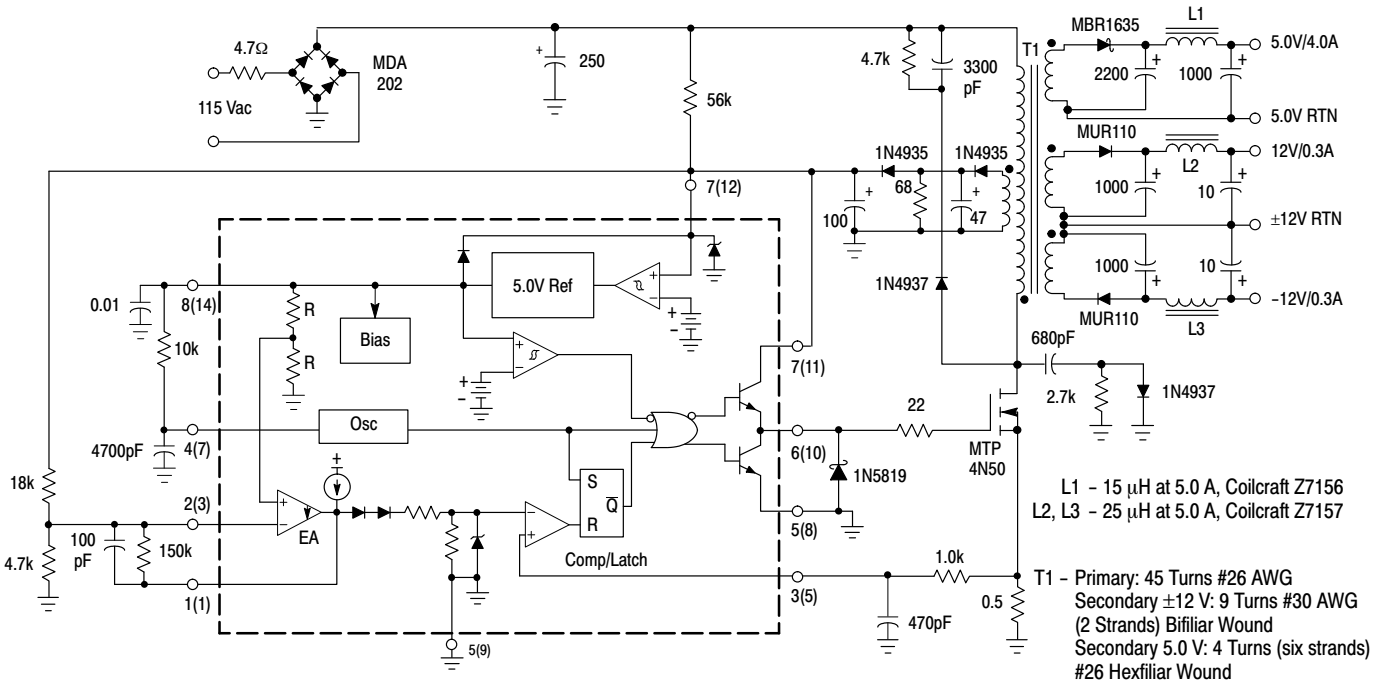
Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 33. Error Amplifier Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 34. Slope Compensation



L1 – 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 – 25 μH at 5.0 A, Coilcraft Z7157

T1 – Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35−3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

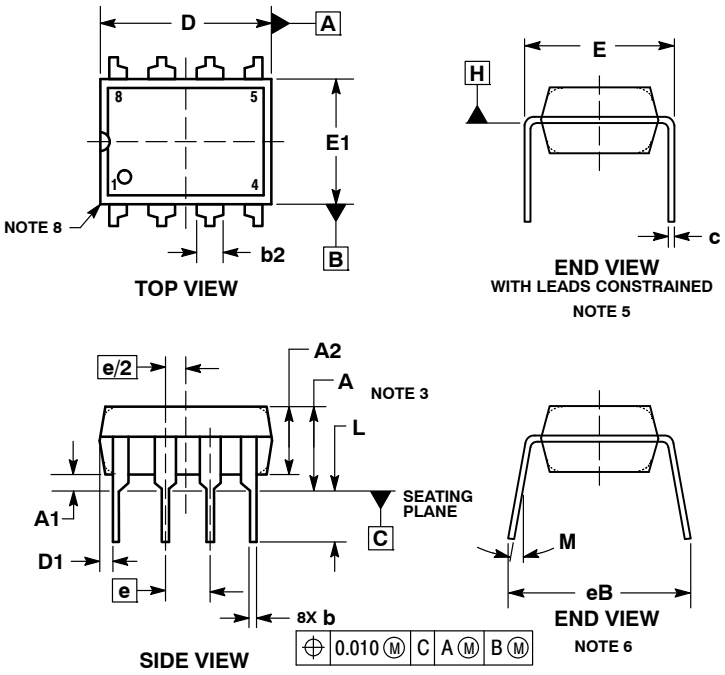
Figure 35. 27 W Off−Line Flyback Regulator

Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted

PACKAGE DIMENSIONS

PDIP–8
N SUFFIX
CASE 626–05
ISSUE N

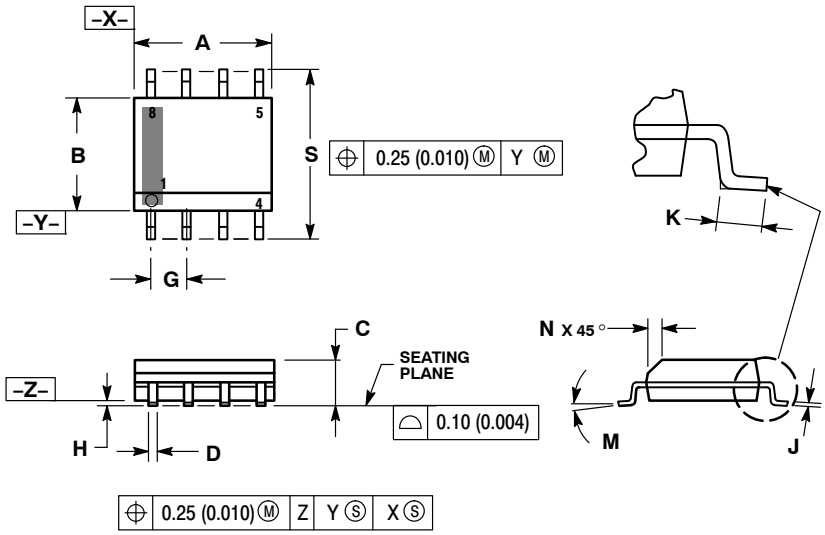


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

PACKAGE DIMENSIONS

SOIC−8
D1 SUFFIX
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244