

## General Description

The WST3427 is the highest performance trench P-ch MOSFET with extreme high cell density , which provide excellent R<sub>DS(on)</sub> and gate charge for most of the small power switching and load switch applications.

The WST3427 meet the RoHS and Green Product requirement with full function reliability approved.

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C<sub>dv/dt</sub> effect decline
- Green Device Available

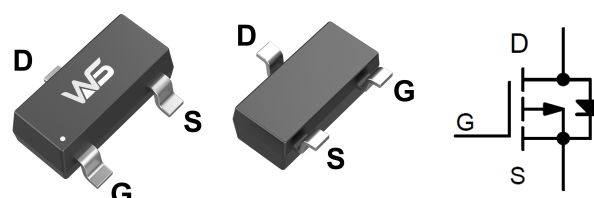
## Product Summary

BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
-20V	140mΩ	-2.5A

## Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

## SOT-23N Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	-20	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub> @T <sub>c</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-2.5	A
I <sub>D</sub> @T <sub>c</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-1.9	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-9.1	A
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup>	1	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJA</sub>	Thermal Resistance Junction-ambient <sup>1</sup>	---	125	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	80	°C/W

**Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^{\circ}\text{C}$ , $I_D=-1mA$	---	-0.016	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-4.5V, I_D=-2A$	---	140	165	$m\Omega$
		$V_{GS}=-2.5V, I_D=-1A$	---	165	210	
		$V_{GS}=-1.8V, I_D=-1.5A$	---	210	240	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.3	-0.5	-1	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.97	---	mV/ $^{\circ}\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-16V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	-1	$\mu A$
		$V_{DS}=-16V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	-5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 8V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$	---	5.9	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	13.1	26.2	$\Omega$
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-2A$	---	5.0	7.8	nC
$Q_{gs}$	Gate-Source Charge		---	0.62	1.0	
$Q_{gd}$	Gate-Drain Charge		---	1.15	2.0	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-4.5V, R_G=3.3\Omega, I_D=-2A$	---	3.5	8.0	ns
$T_r$	Rise Time		---	20.6	46	
$T_{d(off)}$	Turn-Off Delay Time		---	22	52	
$T_f$	Fall Time		---	9.4	24.8	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	---	300	465	pF
$C_{oss}$	Output Capacitance		---	45	67	
$C_{rss}$	Reverse Transfer Capacitance		---	30	59	

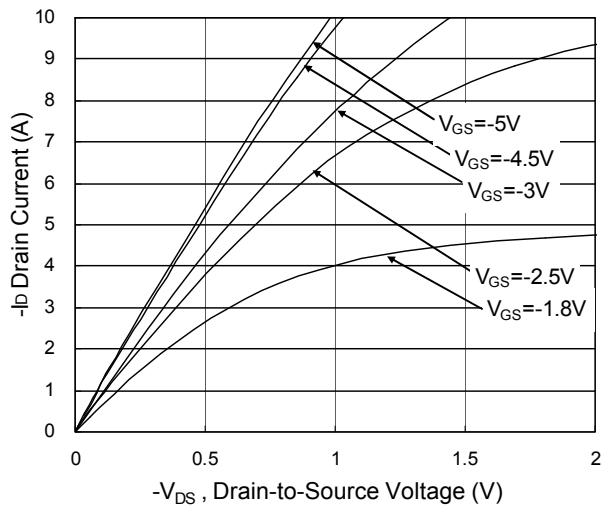
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	-2.5	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	-8	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^{\circ}\text{C}$	---	---	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=-2A, dI/dt=100A/\mu s, T_J=25^{\circ}\text{C}$	---	20	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	4.5	---	nC

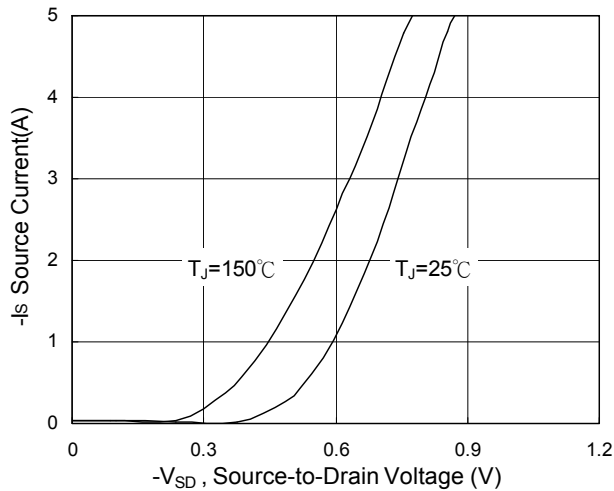
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper,  $t<10\text{sec}$ .
- 2.The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 4.The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

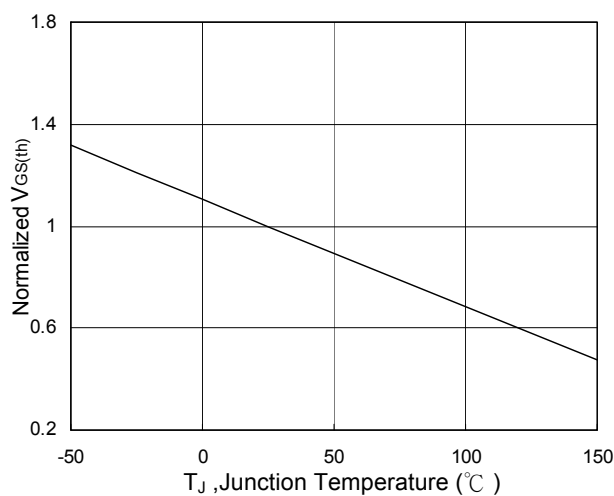
## Typical Characteristics



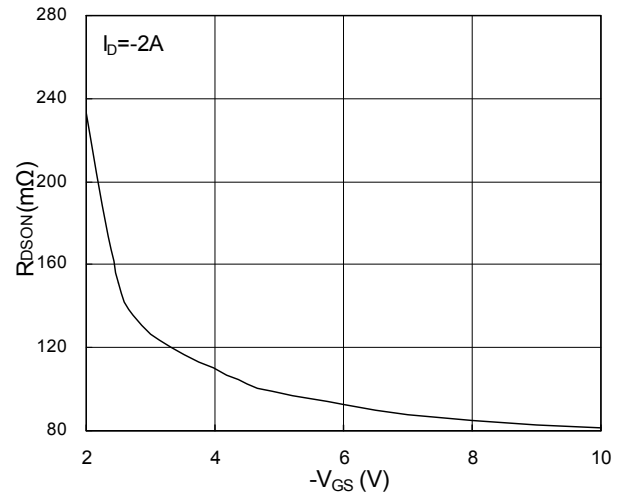
**Fig.1 Typical Output Characteristics**



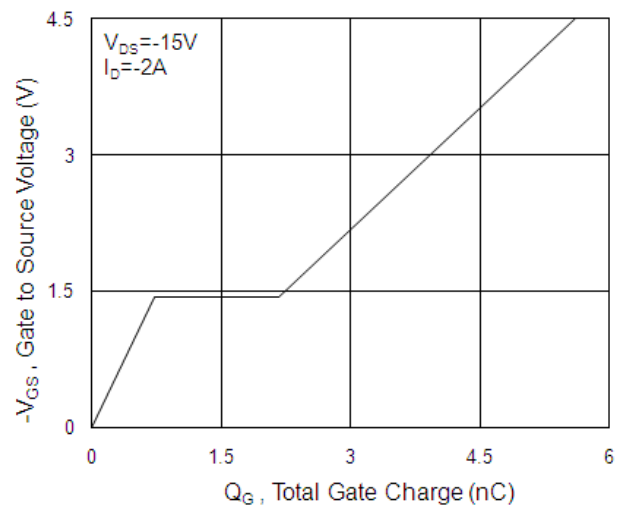
**Fig.3 Forward Characteristics Of Reverse**



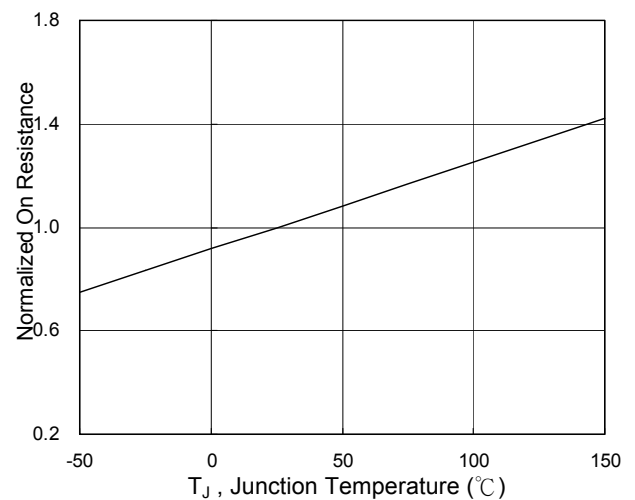
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



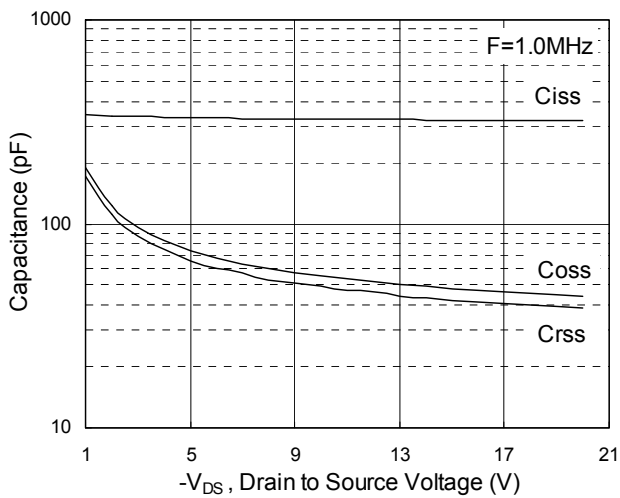
**Fig.2 On-Resistance vs. Gate-Source**



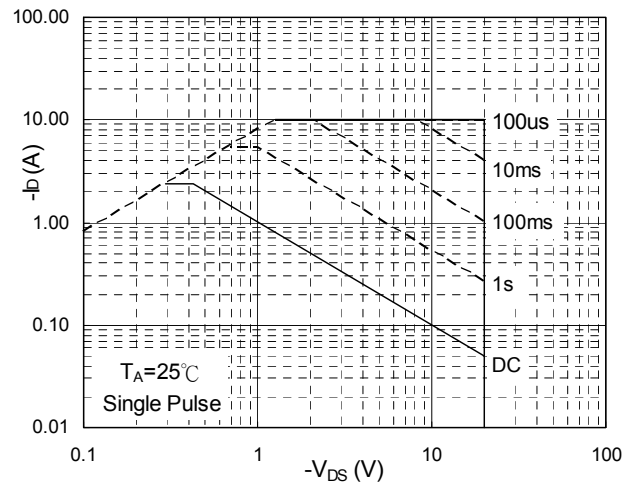
**Fig.4 Gate-Charge Characteristics**



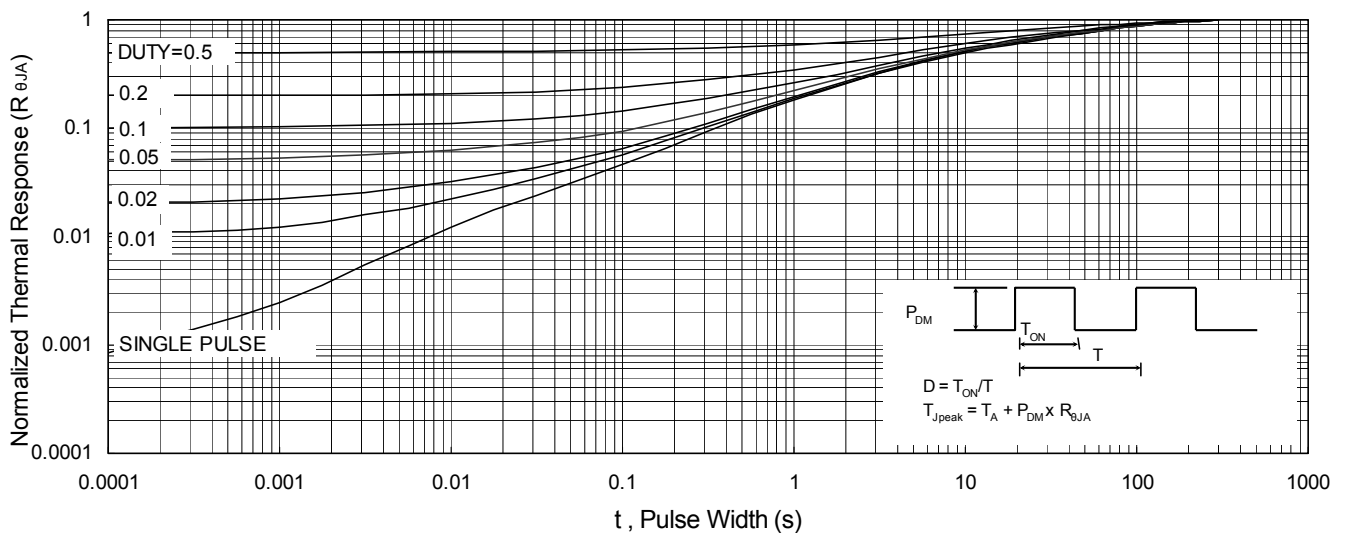
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



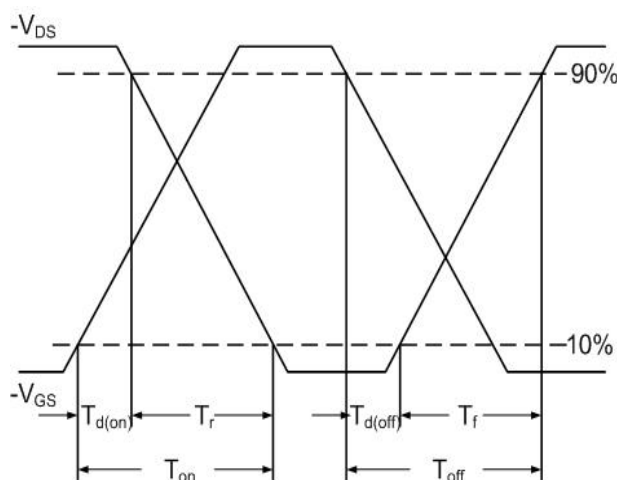
**Fig.7 Capacitance**



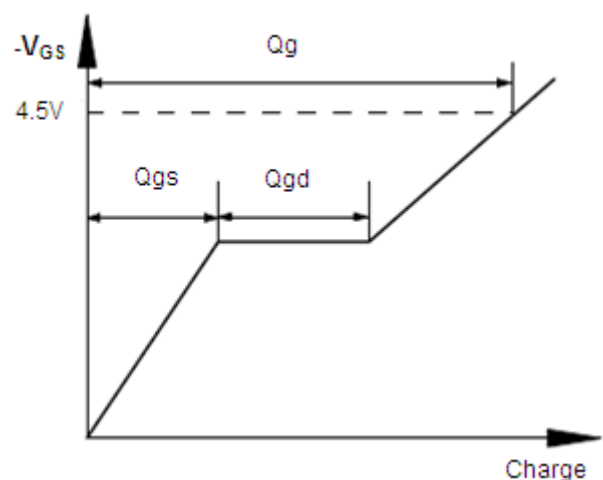
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**

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